

Temperature Behavior

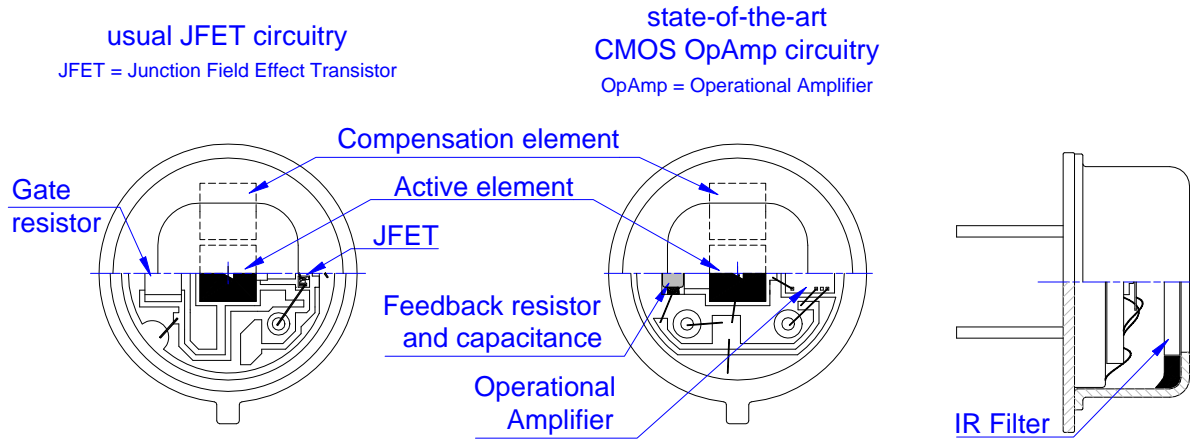


Fig.1 Typical InfraTec Detector Construction

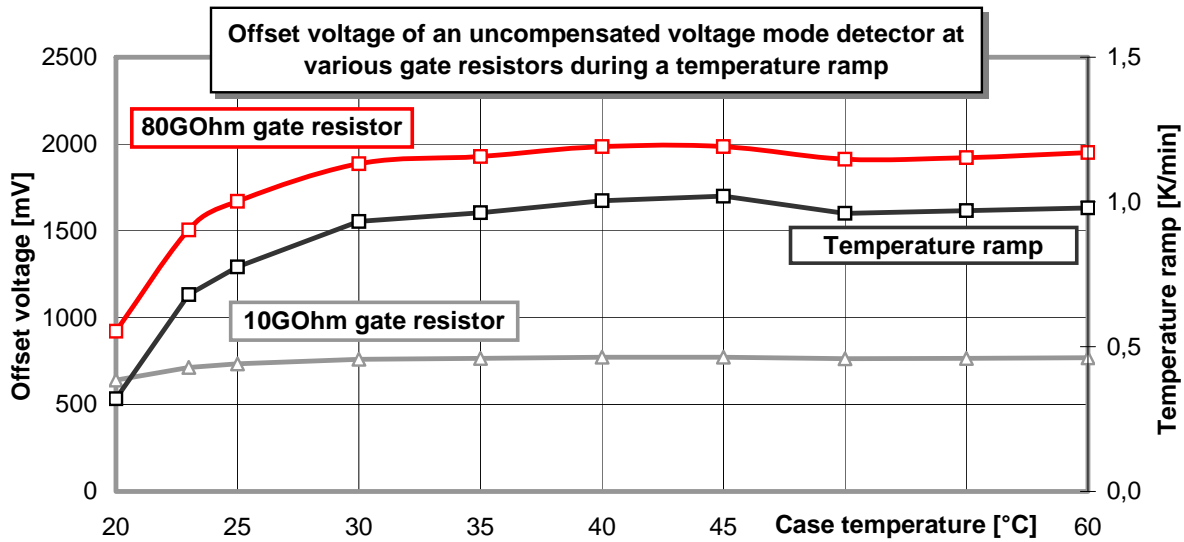


Fig.2 Offset Voltage vs. Temperature at various Gate Resistors (uncompensated voltage mode detector, JFET circuitry)

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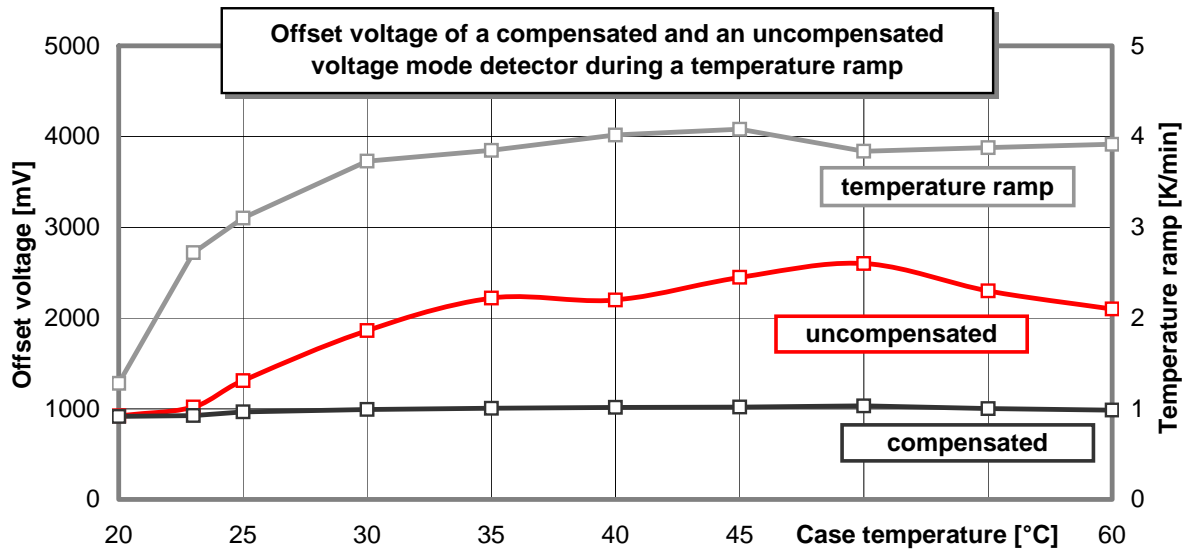


Fig.3 Offset Voltage vs. Temperature (compensated and uncompensated voltage mode detectors, JFET circuitry)

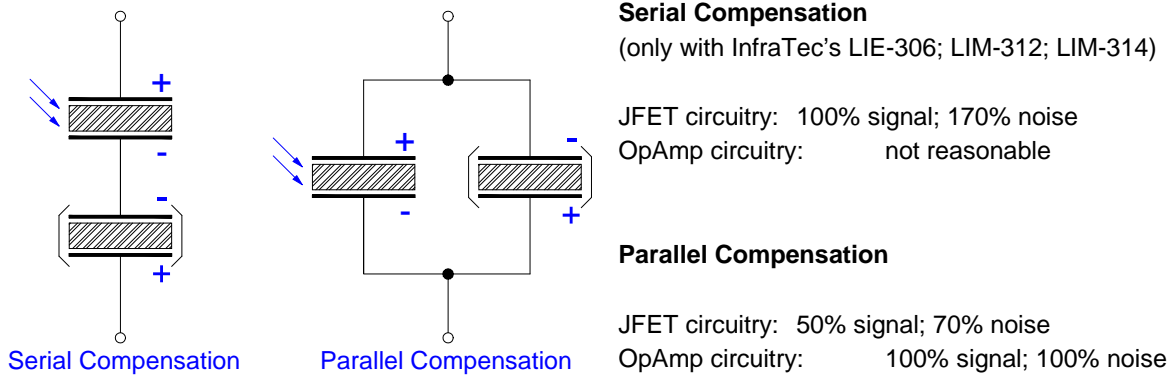


Fig.4 Serial and Parallel Compensation to increase the stability of the DC operating point of pyroelectric detectors in temperature ramps

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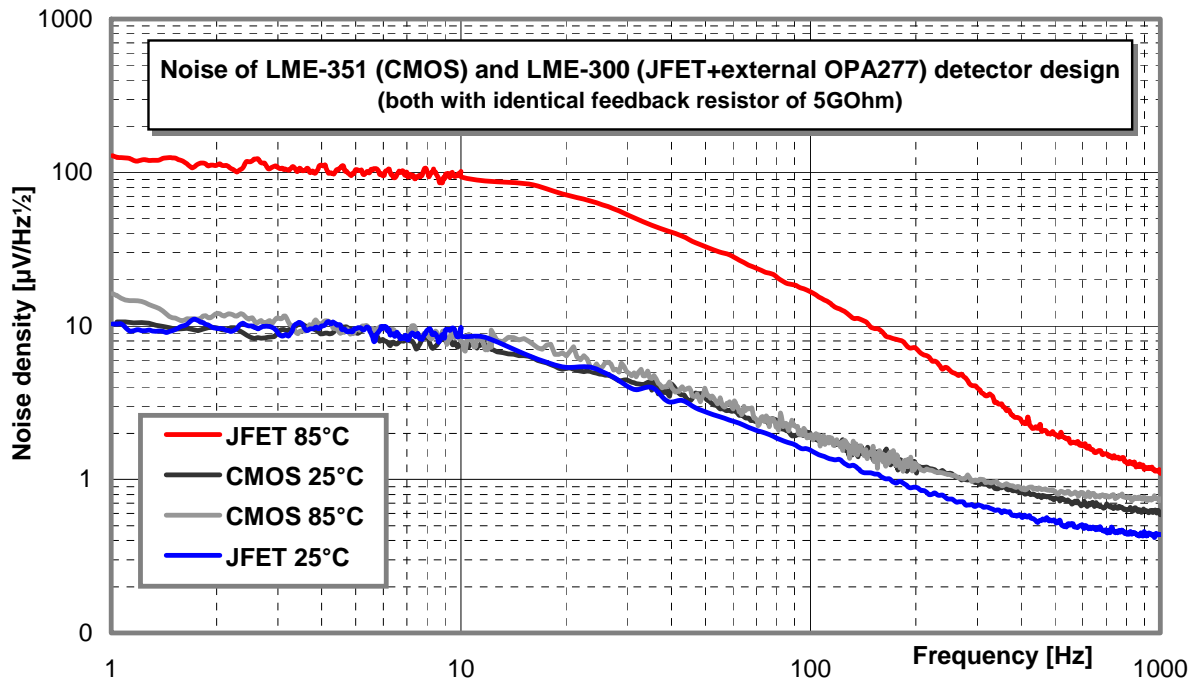


Fig.5 Different behavior of JFET and CMOS input transimpedance amplifiers at temperature increase

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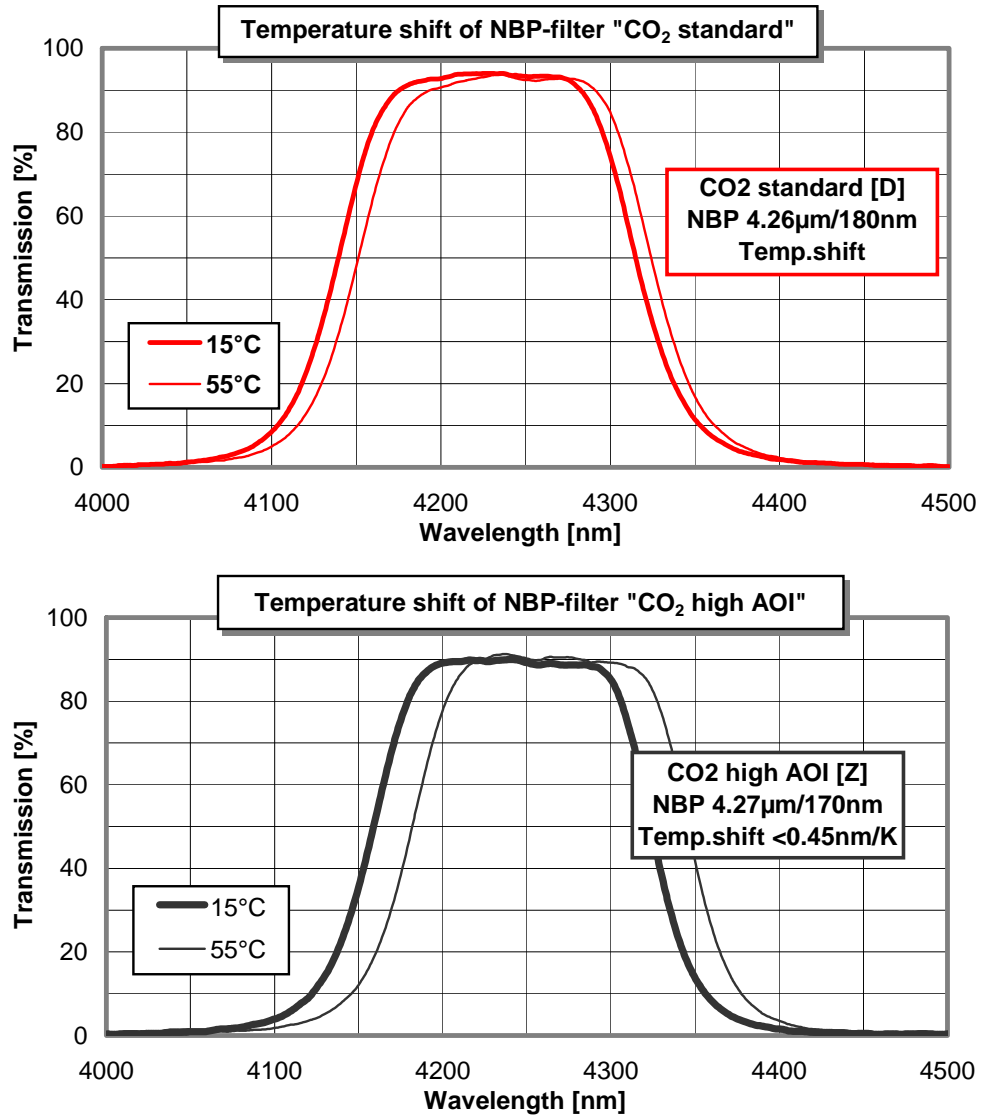


Fig. 6: Temperature Shift of NBP filters with low TC design and without

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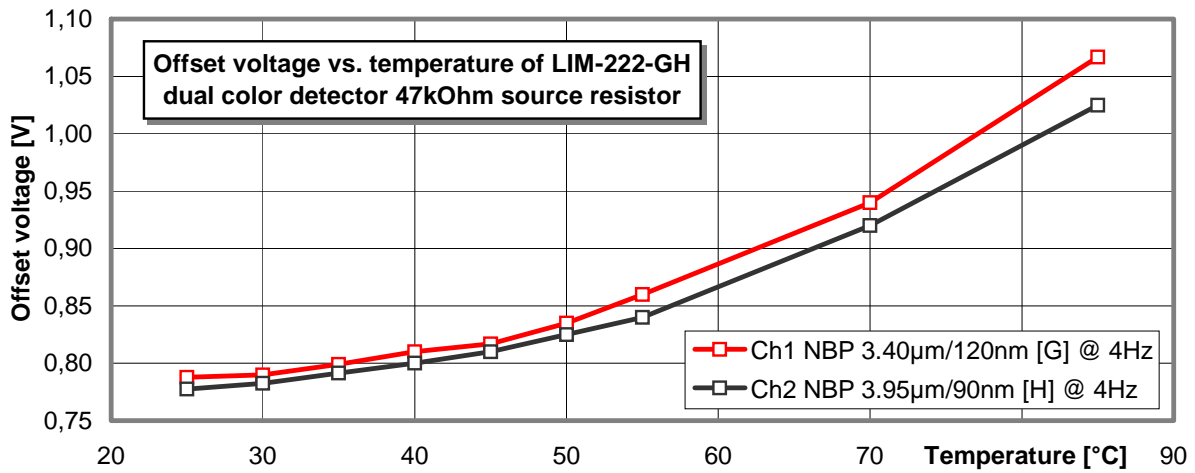


Fig.7 Offset Voltage vs. Temperature (JFET circuitry); after thermal transient period

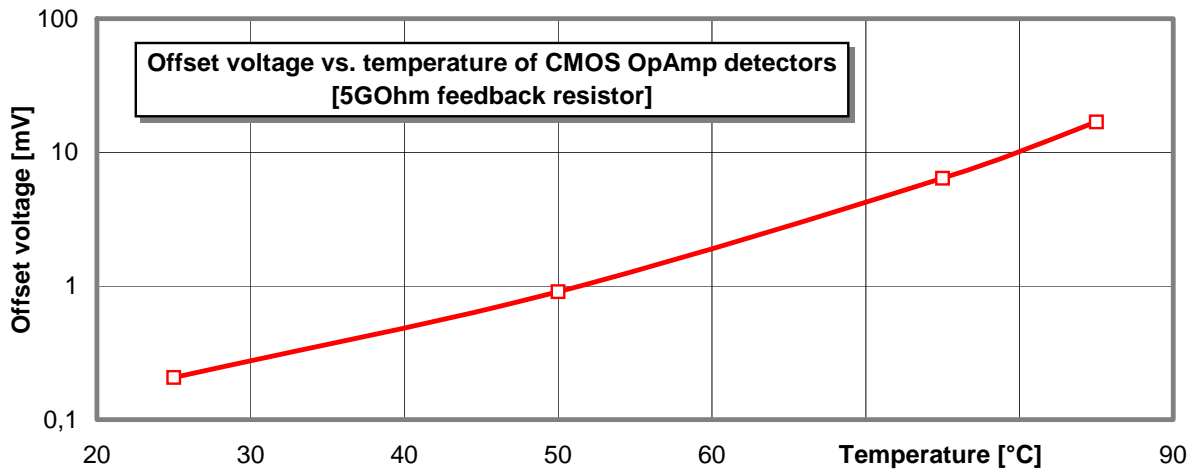


Fig.8 Offset Voltage vs. Temperature (OpAmp circuitry); after thermal transient period

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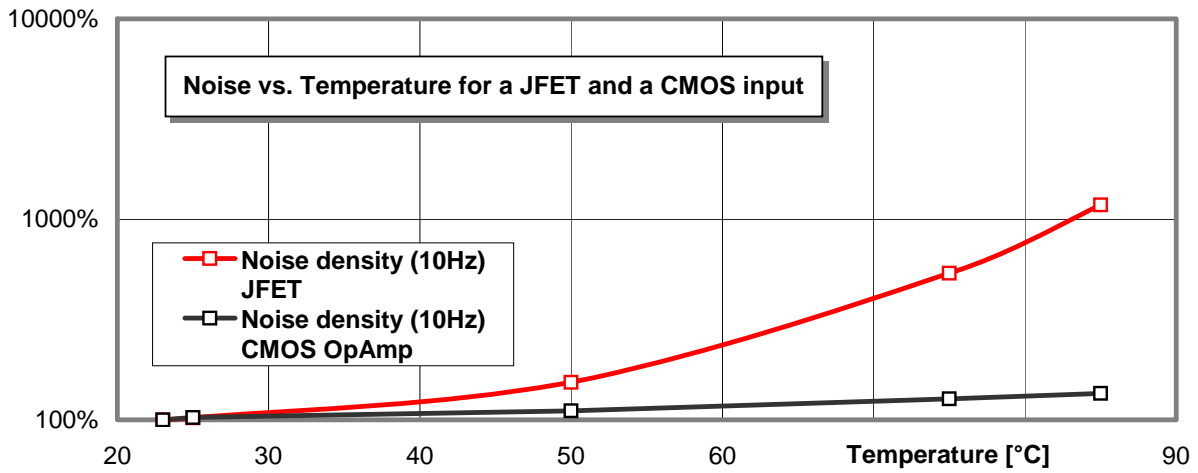


Fig.9 Noise of a JFET and a CMOS OpAmp circuitry at various temperatures

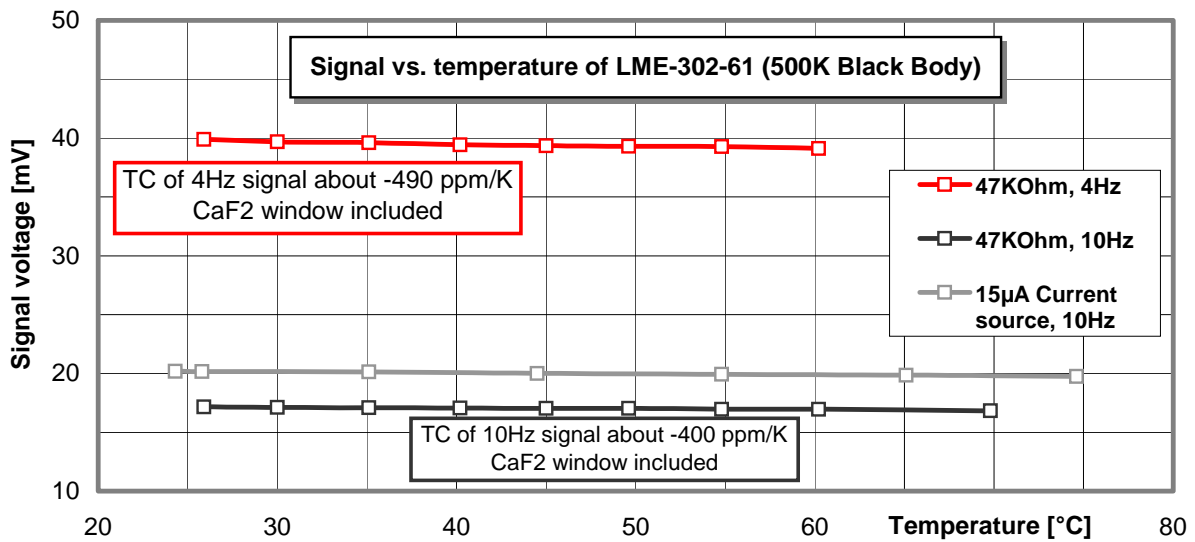


Fig. 10: Signal voltage vs. Temperature at JFET circuitry (LME-302-61: voltage mode with CaF₂ window)

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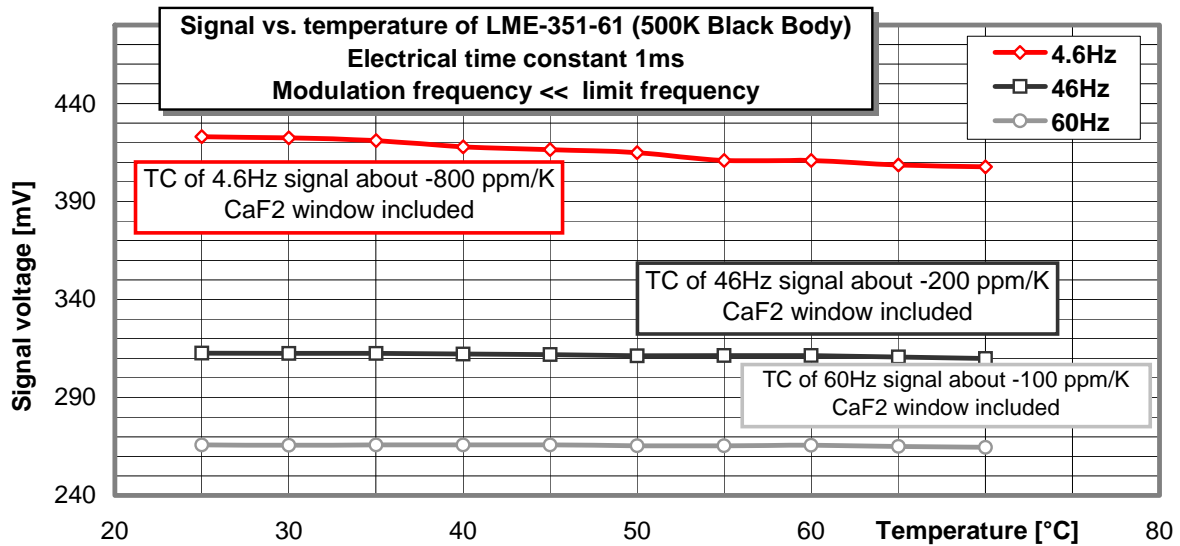


Fig. 11: Responsivity vs. Temperature at OpAmp circuitry (LME-351-DI: current mode with CaF₂ window)

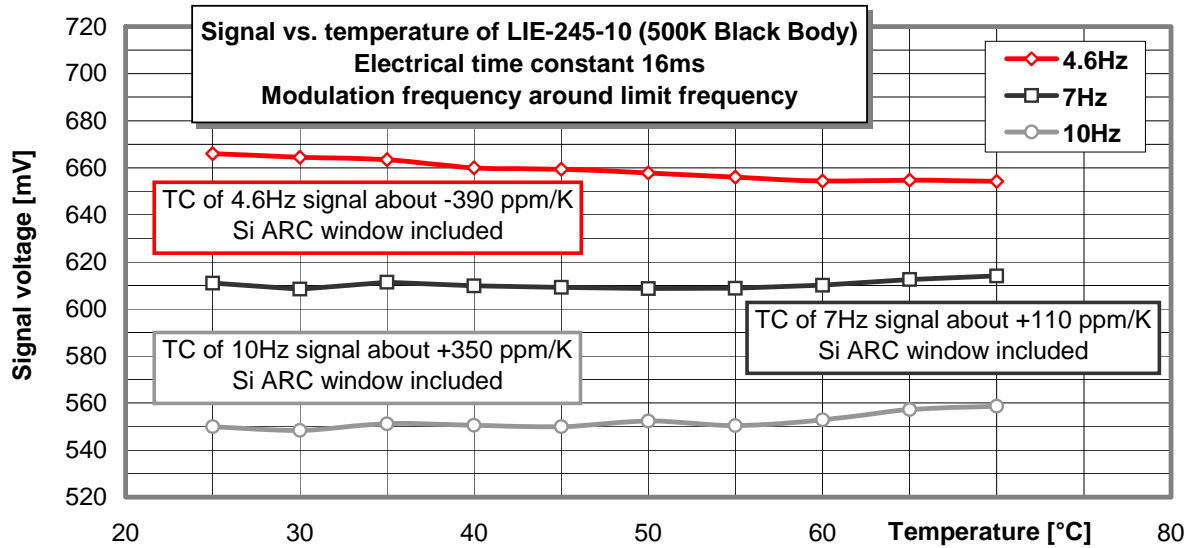


Fig.12 Responsivity vs. Temperature at OpAmp circuitry (LIE-245-10: current mode with Si ARC window)

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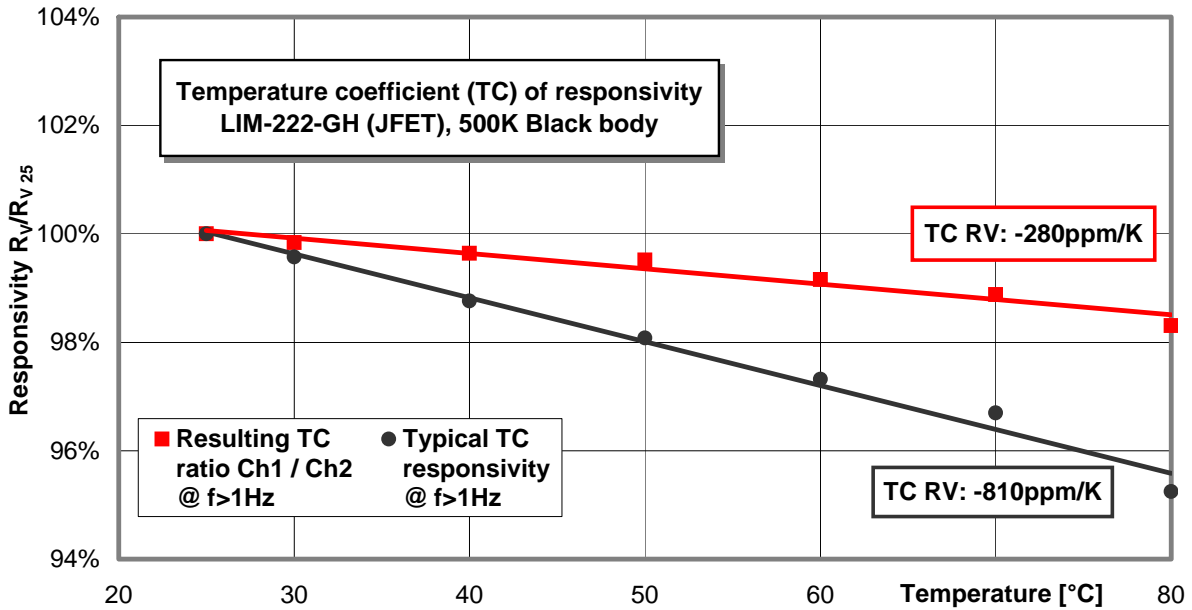


Fig.12: Dual channel detector **LIM-222-GH** (TO39 housing; small chip size; thermal compensation; JFET; voltage mode; ch1: NBP 3.40 μ m / 120nm HC; ch2: NBP 3.95 μ m / 90nm Ref.), IR source 500K black body.

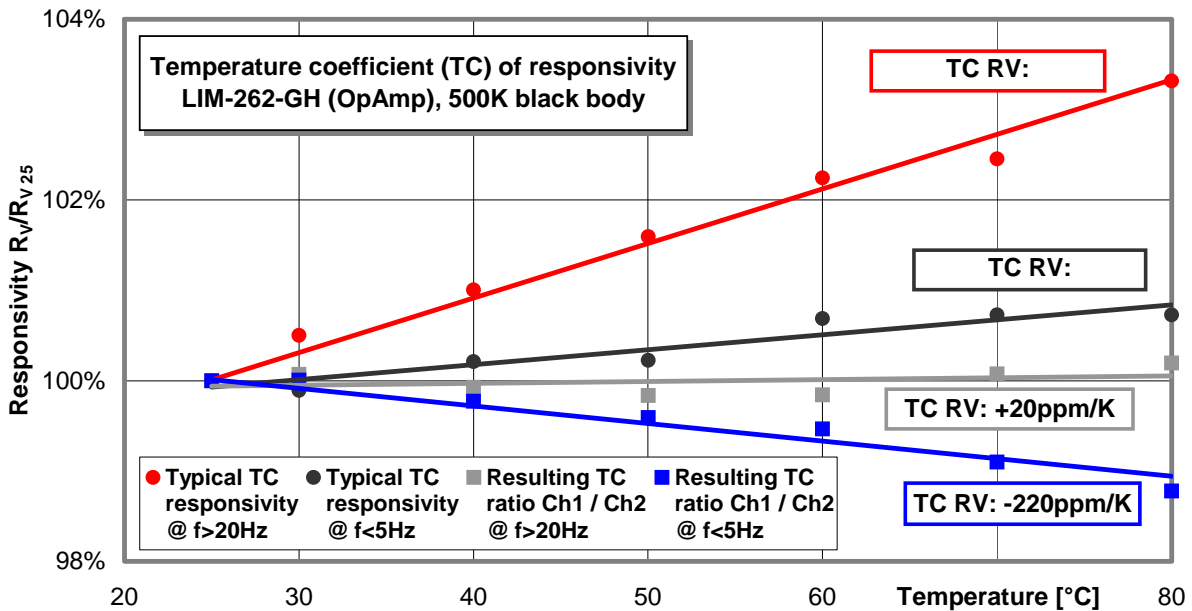


Fig. 13: Dual channel detector **LIM-262-GH** (TO39 housing; small chip size; thermal compensation; OpAmp; current mode; feedback 100GOhm; ch1: NBP 3.40 μ m / 120nm HC; ch2: NBP 3.95 μ m / 90nm Ref.), identical filter placement and IR source as with the LIM-222-GH in Fig.12.

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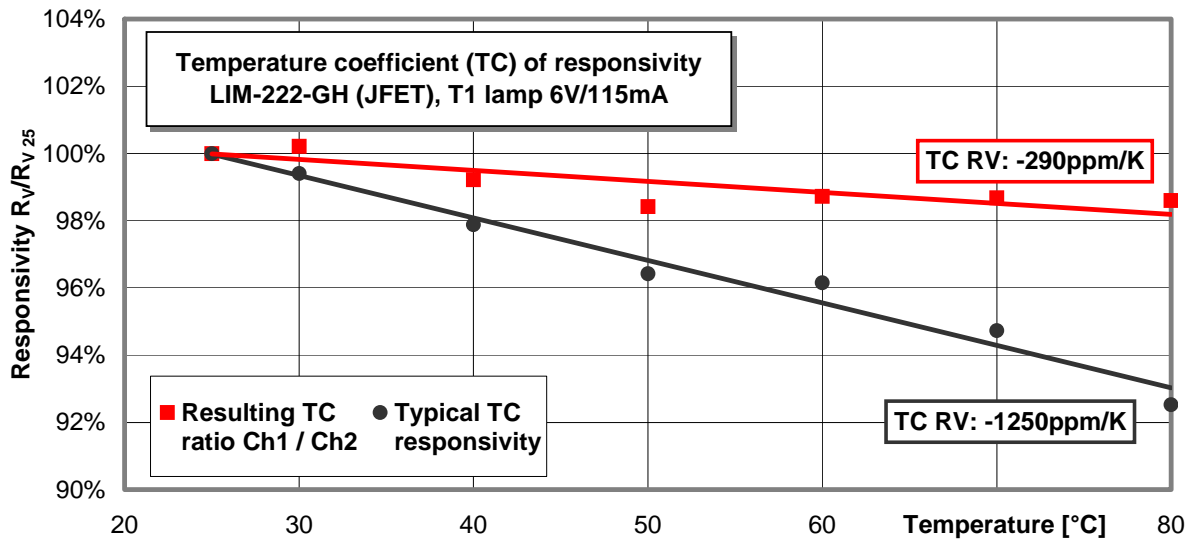


Fig.14: Dual channel Detector **LIM-222-GH** identical to Fig.12 except IR source is a T1 lamp 6V/115mA